CROSS LINK MULTIPLEXER BUS

ABSTRACT OF THE DISCLOSURE

A cross link multiplexer bus comprising a plurality of cross link multiplexers and a plurality of interconnects. The plurality of cross link multiplexers has a destination port configured to receive a signal and an origin port configured to produce the signal. The plurality of interconnects has a set of interconnects coupled between a pair of adjacent cross link multiplexers. Preferably, the destination port is in a first cross link multiplexer, the origin port is in a second cross link multiplexer, and the first cross link multiplexer is configured to convey the signal toward the second cross link multiplexer in more than one direction. In an embodiment, the signal is capable of being represented as a series of characters, and a character is capable of being represented as a number of bits. Preferably, the plurality of cross link multiplexers includes a delay buffer to delay conveyance of a first bit so that it remains substantially synchronized with a second bit. Preferably, the set of interconnects includes a first interconnect to convey the first bit and a second interconnect to convey the second bit. The lengths of the first and the second interconnects are substantially equal.